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Terms	Documents
L2 and ((silicon adj nitride) or (silicon adj carbide) or (silicon adj oxynitride))	5

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L2	L1 and DARC and IMD and (TEOS or FLARE)	5	L2
L1	dual damascene	2240	L1

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L3: Entry 1 of 5 File: USPT Oct 28, 2003

US-PAT-NO: 6638853
DOCUMENT-IDENTIFIER: US 6638853 B1

TITLE: Method for avoiding photoresist resist residue on semioconductor feature sidewalls

DATE-ISSUED: October 28, 2003

INVENTOR-INFORMATION:

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APPL-NO: 10/ 190148 [PALM]
DATE FILED: July 3, 2002

INT-CL: [07] H01 L 21/476

US-CL-ISSUED: 438/633; 438/642, 438/637, 438/640, 438/673
US-CL-CURRENT: 438/633; 438/637, 438/640, 438/642, 438/673

FIELD-OF-SEARCH: 438/633, 438/637-640, 438/672-673, 438/675, 438/692

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	6143646	November 2000	Wetzel	347/20
☐	6287972	September 2001	Ziger et al.	438/637
☐	6372616	April 2002	Yoo et al.	438/592
☐	6420441	July 2002	Allen et al.	204/192.32
☐	6455416	September 2002	Subramanian et al.	438/637

ART-UNIT: 2813

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ABSTRACT:

A method for improving a photolithographic patterning process to avoid undeveloped photoresist contamination in a semiconductor manufacturing process including providing a semiconductor wafer having a process surface including a first anisotropically etched opening extending through a semiconductor wafer thickness portion including an underlying dielectric insulating layer; blanket depositing a polymeric resinous layer over the semiconductor wafer process surface to include filling the first anisotropically etched opening; curing the polymeric resinous layer by exposing the polymeric resinous layer to at least one of thermal or photonic energy to initiate polymer cross linking; chemically mechanically polishing (CMP) the polymeric resinous layer to substantially remove the polymeric resinous layer thickness above the process surface; and, forming a photolithographically patterned photoresist layer over the process surface for forming a second anisotropically etched opening overlying and encompassing the first anisotropically etched opening.

19 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

BRIEF SUMMARY:

1 FIELD OF THE INVENTION

2 This invention generally relates to photolithographic patterning of semiconductor features and more particularly to an improved method for manufacturing semiconductor features such as via-first dual damascene structures while eliminating problems caused by photoresist residue contamination including undeveloped photoresist on via sidewalls.

3 BACKGROUND OF THE INVENTION

4 Since the introduction of semiconductor devices, the size of semiconductor devices has been continuously shrinking, resulting in smaller semiconductor chip size and increased device density. One of the limiting factors in the continuing evolution toward smaller device size and higher density has been the stringent requirements placed on photolithographic processes as line width and step heights have decreased for device features. As one way to overcome such limitations, various methods have been implemented to increase the resolution performance of photoresists and to eliminate photoresist interfering effects occurring in the semiconductor wafer manufacturing process.

5 In the fabrication of semiconductor devices multiple levels may be required for providing a multi-level interconnect structure. During the manufacture of

integrated circuits it is common to place material photoresist on top of a semiconductor wafer in desired patterns and to anisotropically etch away or otherwise remove surrounding material not covered by the resist pattern in order to produce metal interconnect lines or other desired features. During the formation of semiconductor devices it is often required that the conductive layers be interconnected through conduits in an insulating layer. Such conduits are subsequently filled with metal and commonly referred to as vias, which extend through an insulating layer between two conductive areas. Metal interconnecting lines (trench lines) are typically formed over the vias to electrically interconnect the various semiconductor devices within and between multiple levels. The damascene process is a well known semiconductor fabrication method for forming electrical interconnects between levels by forming vias and trench lines.

6 For example, in an exemplary process for forming dual damascene structures, a via opening is first anisotropically etched in an insulating layer also known as an inter-metal dielectric (IMD) layer. The insulating layer is typically formed over a metal or conductive area including an overlying lining or etching stop layer. After a series of photolithographic and anisotropic etching steps forming a respective via opening and overlying trench opening encompassing the via opening, the via opening and the trench opening are filled with a metal (e.g., Al, Cu) to form via and trench line portions of a dual damascene structure. The excess metal above the trench level is then removed by well known chemical-mechanical polishing (CMP) processes.

7 As feature sizes in anisotropic etching process have diminished, photolithographic patterning processes require activating light (radiation) of increasingly smaller wavelength. Increasingly, deep ultraviolet (DUV) photoresists with activating light source wavelengths of less than about 250 nm, for example, from about 193 nm to about 248 nm are used. Exemplary DUV photoresists, for example, include PMMA and polybutene sulfone.

8 One problem affecting DUV photoresist processes has been the interference of residual nitrogen-containing species, for example amides, with the DUV photoresist. Residual nitrogen-containing contamination is one of the greater concerns in the use of metal nitride layers such as silicon nitride and silicon oxynitride and metal carbide layers such as silicon carbide. For example, such layers are frequently used as a etching stop layers and silicon oxynitride as a dielectric anti-reflectance coating (DARC). The nitride layers are frequently formed by CVD process using amine and amide containing precursors which tend to diffuse into adjacent porous layers. For example, the increasing use of low-k dielectric materials, typically having a high degree of porosity, facilitates absorption and transport of contaminating chemical species. For example, it is believed that nitrogen radicals created due to the presence of nitrogen containing species, such as amines and amides, interfere with chemically amplified photoresists, for example DUV photoresists, by neutralizing the acid catalyst, thereby rendering the contaminated portion of the photoresist insoluble in the developer. As a result, residual photoresist may remain on patterned feature edges, sidewalls, or floors of features, affecting subsequent etching or metal filling processes leading to, for example, electrical open circuits or increased resistivity.

9 In a via-first dual damascene process, a method is disclosed for forming a via plug at least partially filling the via opening in commonly assigned co-pending application Ser. No. 10/035,690, filed Nov. 8, 2001, which is incorporated herein by reference. For example, following formation of a via opening, a via plug of polymeric material is formed by depositing an resinous layer, for example an I-line resin, to fill the via opening. The via plug is formed to at least partially fill the via opening by a plasma etch back

process of the resinous layer. The via plug is intended to prevent out diffusion of contaminating species from the IMD layer to contaminate subsequently deposited DUV photoresist for trench line opening patterning. A shortcoming of the etchback process is the difficulty in forming a via plug fully filling the via opening due to the difficulty in determining etching endpoint thereby frequently forming a partially filled via opening. Another shortcoming is the via sidewalls may be damaged during the etchback process. For example, the DUV photoresist layer used for patterning the trench openings, fills the upper portion of the via opening and forms an undeveloped photoresist residue layer along a portion of the sidewalls above the via plug of the via opening during the photolithographic patterning process. The photoresist residue is believed to be caused by contaminating chemical interference (e.g., amides or amines) with the DUV photoresist exposure and development process. As a result, the upper portions of the via sidewalls above the via plug are contaminated with an undeveloped photoresist residue layer, also referred to as photoresist poisoning, which subsequently detrimentally affects etching profiles, for example, in etching the trench portion of the dual damascene structure. Consequently, subsequent metal filling processes for filling the dual damascene structure with metal, for example copper, results in poor step coverage. As a result, areas of high electrical resistance are formed thereby leading to electrical reliability problems in semiconductor devices including the formation of open circuits.

10 Other approaches to prevent the diffusion of contaminating nitrogen containing species from overlying etching stop or DARC layers including for example silicon oxynitride, include forming a silicon dioxide layer over the low dielectric constant IMD layer prior to forming the etching stop or DARC layers. A shortcoming of this approach is the added stresses applied to the IMD layer and the added contribution to the overall capacitance of the multi-level semiconductor device.

11 There is therefore a need to develop a method whereby reliable photolithographic processes may be carried out without the detrimental effects of photoresist poisoning.

12 It is therefore an object of the invention to provide a method in the semiconductor processing art whereby reliable photolithographic processes may be carried out without the detrimental effects of photoresist poisoning while overcoming other shortcomings and deficiencies in the prior art.

13 SUMMARY OF THE INVENTION

14 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a method for improving a photolithographic patterning process to avoid undeveloped photoresist contamination in a semiconductor manufacturing process.

15 In a first embodiment, the method includes providing a semiconductor wafer having a process surface including a first anisotropically etched opening extending through a semiconductor wafer thickness portion including an underlying dielectric insulating layer; blanket depositing a polymeric resinous layer over the semiconductor wafer process surface to include filling the first anisotropically etched opening; curing the polymeric resinous layer by exposing the polymeric resinous layer to at least one of thermal or photonic energy to initiate polymer cross linking; chemically mechanically polishing (CMP) the polymeric resinous layer to substantially remove the polymeric resinous layer thickness above the process surface; and, forming a

photolithographically patterned photoresist layer over the process surface for forming a second anisotropically etched opening overlying and encompassing the first anisotropically etched opening.

DRAWING DESCRIPTION:

These and other embodiments, aspects and features of the invention will become better understood from a detailed description of the preferred embodiments of the invention which are described below in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A-1G are representative cross sectional side views of a portion of a semiconductor wafer including a dual damascene structure at stages in the manufacturing process according to the present invention.

FIG. 2 is a representative process flow diagram including embodiments of the present invention.

DETAILED DESCRIPTION:

1 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

2 Although the present invention is explained with reference to a dual damascene process, it will be appreciated that the present invention may be adapted to the formation of any anisotropically etched semiconductor, where the photolithographic patterning of a second feature overlying the first feature advantageously avoids the accumulation of undeveloped photoresist contamination within the underlying first feature including at least a sidewall portion.

3 In a first embodiment of the present invention, a first anisotropically etched semiconductor feature opening formed in a dielectric insulating layer is provided. A polymeric resinous layer is blanket deposited over the insulating layer to fill the anisotropically etched semiconductor feature including a curing process. The excess polymeric resinous layer is then subjected to a chemical mechanical polishing (CMP) process to remove the polymeric resinous layer to the semiconductor feature opening level. A second semiconductor feature is then photolithographically patterned for anisotropic etching overlying and encompassing the first anisotropically etched semiconductor. feature

4 In one embodiment according to the present invention, the semiconductor feature opening is a via opening. For example, the via opening is created as a step in a via first dual damascene process whereby a trench opening is subsequently formed overlying and encompassing the via opening, the trench opening being anisotropically etched to include etching a portion of the via opening.

5 In other embodiments, the dielectric insulating layer also referred to as an inter-metal dielectric (IMD) layer includes at least an overlying dielectric anti-reflectance coating (DARC) layer. For example, the DARC layer is preferably silicon oxynitride (e.g., SiON) but may include other nitride DARC

layers such as titanium nitride (e.g., TiN). Less preferably, the DARC layer may include an underlying etching stop layer, for example, formed of silicon nitride or silicon carbide. Also less preferably, the DARC layer may include an underlying silicon dioxide capping layer, for example, formed of TEOS by a conventional PECVD method to block nitrogen containing species diffusion into the IMD layer originating from overlying nitride layers including the DARC layer. Such silicon dioxide capping layers are less preferred since they increase the overall capacitance of the semiconductor device.

6 Preferably, the CMP process removes the polymeric resinous layer to the via opening level, in other words, the CMP process reveals the DARC layer. Preferably, following the oxide CMP process the via opening remains substantially filled with the polymeric resin. By the term `substantially filled`, is meant the via opening is at least 90 percent filled. More preferably, the semiconductor feature is completely filled, neglecting CMP dishing effects at the central portion of the opening.

7 Preferably the CMP process is a conventional oxide CMP process. For example, an oxide polishing slurry, for example, includes abrasive particles having at least one of silica (SiO.sub.2), alumina (Al.sub.2 O.sub.3), ceria (CeO.sub.2), titania (TiO.sub.2), manganese oxide (MnO.sub.2), and zirconia (ZrO.sub.2). Typically, the abrasive content of the slurry is about 1 weight percent to about 20 weight percent, more preferably, about 5 to about 10 weight percent. Further, the metal oxides typically have a mean particle diameter (i.e., meaning primary particles and agglomerates of primary particles) ranging from about 20 nanometers to about 500 nanometers, more preferably, about 100 to about 300 nanometers. For example, some slurry mixtures require appropriate surfactant additives to inhibit particle agglomeration as is known in the art. In an exemplary embodiment of the invention, for example, using a typical silica slurry, the material removal rate of the polymeric resinous layer was about 56,000 Angstrom per minute while the removal rate of an underlying silicon oxynitride DARC layer was from about 500 to about 600 Angstroms per minute thereby providing good CMP selectivity contrast to prevent DARC layer overpolishing.

8 For example, in an exemplary embodiment, referring to FIG. 1A-1G, are shown cross sectional side views of a portion of a multi-level semiconductor device at stages in manufacturing a dual damascene structure. Referring to FIG. 1A is shown is a conductive region 10, for example, copper, formed in a dielectric insulating layer 11A having an overlying etching stop layer 11B, for example silicon nitride or silicon carbide. The etching stop layer is formed by a conventional chemical vapor deposition (CVD) process including for example, PECVD (plasma enhanced CVD), LPCVD (low pressure CVD), or HDPCVD (high density plasma CVD) having a thickness of about 200 Angstroms to about 1000 Angstroms.

9 Formed over the etching stop layer 11B is insulating dielectric layer 12 also referred to as an inter-metal dielectric (IMD) layer formed of, for example, a low-k (low dielectric constant) carbon and/or fluorine doped silicon dioxide as is known in the art. Typically, the dielectric constant of the IMD layer is less than about 3.0. It will be appreciated that a silicon dioxide layer, formed by for example, a PECVD process using Tetra-ethyl-orthosilicate (TEOS) may be first formed over the etching stop layer prior to forming of the IMD layer to block diffusion of nitrogen containing species into the IMD layer, but is not a most preferred method since the added silicon dioxide layer undesirably increases the overall capacitance. In addition, the method of the present invention advantageously makes the formation of such capping or blocking layers unnecessary since the via opening is formed with a polymeric resinous material substantially filling the via opening thereby blocking out diffusion of any contaminating nitrogen species, such as amines, from the IMD

layer to interfere with photoresist in a photolithographic patterning process.

10 It will be appreciated that other low-k materials may be used for the IMD layer and that the method according to the present invention is likewise applicable to those materials where the materials include interconnecting pores such that amide or amine contain species may diffuse therethrough. For example, the interconnecting pores have a mean diameter of greater than about 3 Angstroms. Exemplary low-k inorganic materials include, for example, porous oxides, xerogels, or SOG (spin-on glass). For example the IMD layer is formed having a thickness of from about 3000 Angstroms to about 10000 Angstroms by a conventional plasma enhanced chemical vapor deposition process (PECVD), HDP-CVD, or spin on process for SOG.

11 A metal nitride etching stop layer 14 also preferably functioning as a dielectric anti-reflectance coating (DARC) to reduce undesired light reflections in subsequent photolithographic patterning processes, is deposited over the IMD layer 12. The etching stop/DARC layer 14 is preferably formed of silicon oxynitride (e.g., SiON) but may include other nitride DARC materials such as titanium nitride. The silicon oxynitride layer 14 is deposited by a conventional chemical vapor deposition (CVD) process including for example, PECVD (plasma enhanced CVD), LPCVD (low pressure CVD), or HDPCVD (high density plasma CVD) by reacting silane (SiH.sub.4) and nitrogen, including nitrogen containing precursors, with oxygen under conditions that are well known in the art. It will be appreciated that a separate etching stop layer overlying the IMD layer 12, for example, silicon nitride (e.g., Si.sub.3 N.sub.4) together with an overlying DARC layer of silicon oxynitride may also be suitably used in place of a silicon oxynitride etching stop layer 14, however a single silicon oxynitride layer is more preferable to minimize capacitance contributions and processing cycles. The silicon oxynitride layer 14 is preferably formed having a thickness of about 200 to about 1000 Angstroms.

12 Still referring to FIG. 1A, a photoresist layer 16 is next deposited over the etching stop layer 14 and exposed and developed according to a conventional photolithographic patterning process to form an anisotropic etching pattern for via openings, for example, via opening pattern 18. Preferably, a deep ultraviolet (DUV) photoresist is used for patterning the via openings including an activating radiation source with a wavelength of less than about 250 nm, for example, from about 193 nm to about 250 nm, to expose the photoresist layer 16. The photoresist layer 16 may be any conventional DUV photoresist layer including a bi-layer photoresist including, for example, a chemically amplified resist including a photogenerated acid. There are several suitable commercially available DUV photoresists known in the art.

13 Referring to FIG. 1B, via opening 20 is anisotropically etched through the thickness of the etching stop/DARC layer 14, the IMD layer 12, and the etching stop layer 11B to create via opening 20 in closed communication with underlying conductive region 10. The anisotropic etching is carried out by conventional plasma reactive ion etch (RIE) processes including for example, mixtures of hydro-fluorocarbons, fluorocarbons, oxygen, and nitrogen.

14 Referring to FIG. 1C, after removing the photoresist layer 16 by either a wet chemical stripping process or preferably a plasma ashing process including oxygen as is known in the art, a curable polymeric resinous layer 22, preferably an I-line resin such as a novolac resin, is blanket deposited, for example by a conventional spin-coating process, over the etching stop layer 14 to fill the via opening 20. By the term `curable` is meant a polymer including at least one of a photosensitive and thermal agent for initiating polymeric cross-linking reactions. Most preferably, the curable polymeric resin is an I-line novolac resin. Preferably, the curable polymeric resin has a weight

average molecular weight of from about 10,000 to about 90,000 to provide increased resistance to nitrogen-containing species diffusion across the via sidewalls and to give increased dimensional stability in a subsequent CMP process.

15 Referring to FIG. 1D, following blanket deposition, the polymeric resinous layer 22 is preferably subjected to a curing process including for example, a conventional thermal curing process at temperatures for example, from about 100.degree. C. to about 160.degree. C. to initiate polymer cross-linking. It will be appreciated that the curing time will depend on the polymeric resin and thermal sensitizing agent for initiating polymeric cross linking reactions. For example, for an I-line novolac resin, a thermal curing time of from about 5 minutes to about 20 minutes at temperatures from about 100.degree. C. to about 160.degree. C. is a suitable thermal curing process. The curing process may optionally include a photocuring process, the wavelength and time of exposure depending on the photosensitive curing agent included in the polymeric resin. It will be appreciated that other polymeric resins may be used, for example, including at least one of aliphatic urethane acrylates; aliphatic urethane diacrylates; aliphatic urethane triacrylates; hexafunctional aliphatic urethane acrylates; hexafunctional aromatic urethane acrylates; trifunctional aromatic urethane acrylates, aromatic urethane acrylates; urethane methacrylates; epoxy acrylates; epoxy methacrylates; polybutadiene dimethylacrylates; diacrylates of bisphenol-A epoxy resins; modified bisphenol-A epoxy acrylate resins; novolac epoxy acrylates; modified epoxy acrylates; partially acrylated bisphenol-A epoxy resins; bisphenol-A epoxy diacrylates; polyester resins; cycloaliphatic epoxide resins; modified cycloaliphatic epoxides; aliphatic polyols; partially acrylated bisphenol-A epoxy resins; and cycloaliphatic diepoxides.

16 In one embodiment of the present invention, following curing of the polymeric resinous layer 22, a CMP process is carried out to remove the excess polymeric resinous layer 22 overlying the via opening level to reveal the DARC layer and form via plug 22B substantially filling the via opening 20. Preferably, a conventional oxide CMP process as outlined above is performed. Preferably, the CMP process is carried out at least to endpoint detection. For example, suitable endpoint detection means include real-time optical detection methods including wafer polishing surface reflectance measurements, as well as laser interferometry. In addition, methods such as polishing pad motor load monitoring, or monitoring the electrical potential of the polishing effluent may be suitably used for endpoint detection. Optionally, a second curing process including at least one of a thermal and photo curing process may be carried out following the CMP process.

17 Referring to FIG. 1E, following via plug formation, a photoresist layer 26 (trench line photoresist) is deposited over the etching stop/DARC layer 14 and photolithographically patterned by exposure and development to form a trench opening pattern 26B for anisotropically etching a trench line opening overlying and encompassing via plug 22B. Preferably the photoresist is a DUV photoresist designed for exposure at a wavelength less than about 250 nm, for example about 193 nm to about 250 nm, as discussed with reference to via photoresist layer 16 in FIG. 1A.

18 Referring to FIG. 1F, a conventional anisotropic etching process (e.g., RIE) is then carried out to first etch through the etching stop/DARC layer 14. According to another embodiment of the present invention, an RIE process having a fluorine rich plasma etching chemistry, preferably using a plasma with a carbon to fluorine ratio of at least about 4, is used to anisotropically etch through a thickness portion of the IMD layer 12 including etching through a portion of via plug 22B to complete the formation of trench

opening 28. The fluorine rich etching chemistry is used to minimize additional formation of polymeric residues on the trench opening and via sidewalls.

19 Referring to FIG. 1G, following the trench line etching process, the trench line opening is completed by removing the trench line photoresist layer 26 and remaining via plug 22B from the via opening 20 to form the via portion 20 and trench line portion 28 of the dual damascene structure. Preferably, a conventional plasma ashing process in an oxygen containing plasma is used; however, a wet chemical striping process as is known in the art may be suitably used as well. The dual damascene structure is typically completed by forming an adhesion/barrier layer of for example, tantalum nitride (TaN)(not shown) over the floor and sidewalls of the trench line opening 28 and via opening 20 followed by filling with a metal, for example copper, and planarizing with a chemical mechanical polishing (CMP) process (not shown).

20 Referring to FIG. 2, is shown a process flow diagram including several embodiments of the present invention. It will be understood that whenever reference herein is made to the singular of a semiconductor feature, for example, a via opening, that such reference includes a plurality of structures included in a semiconductor wafer. In addition it will be understood that multi-levels of semiconductor features are formed in sequential order to form a multi-level semiconductor device, thereby requiring repeating the process steps a number of times to complete formation of a semiconductor device.

21 According to several embodiments of the present invention, included in process 201, a first anisotropically etched opening in an insulating dielectric layer, for example a via opening in a via first dual damascene process, is provided. In process 203, a polymeric resinous layer, is blanket deposited to fill the via opening followed by a thermal curing process to initiate polymer cross-linking. In process 205 the polymeric resinous layer above the via level is removed by a CMP process to reveal the DARC layer and form a via plug substantially filling the via opening. In process 207 a DUV photoresist layer is provided over the via opening, for example, a chemically amplified photoresist, and photolithographically patterned for anisotropically etching a second semiconductor feature, for example, a trench line opening overlying and encompassing the via opening.

22 In process 209, a trench line opening is anisotropically etched through the etching stop/DARC layer and a thickness portion of the dielectric insulating layer (IMD layer) the etching chemistry for etching through the IMD layer preferably including a fluorine rich etching chemistry.

23 In process 211, the DUV photoresist layer including the via plug is removed according to at least one of a conventional plasma ashing process or a conventional wet chemical stripping process.

24 The dual damascene structure is then completed by conventional processes (not shown) including, for example, depositing an adhesion/barrier layer and filling the dual damascene structure with a metal, for example copper, followed by a metal CMP process to remove excess material above the etching stop layer.

25 Thus, the method according to the present invention provides a method whereby a photolithographic patterning process in, for example, forming a dual damascene structure may be reliably carried out without the detrimental effects of photoresist poisoning caused by undeveloped photoresist remaining on semiconductor features. In one embodiment, the method of the present invention prevents the formation of etching resistant polymeric residue

including photoresist on the sidewalls of via openings thereby detrimentally affecting the formation of an overlying trench feature. The formation of the via plug substantially filling the via opening according to a CMP planarization process according to an embodiment of the present invention operates to block the out diffusion of nitrogen containing photoresist contaminating species to interfere with subsequent trench line patterning and anisotropic etching. In contrast with the prior art process of etching back the polymeric resinous layer to form the via plug, the difficulties of overetching and via sidewall damage are avoided. Further, the necessity of adding silicon dioxide capping layers to protect the IMD layer from contaminating nitrogen containing species is avoided thereby avoiding an increase to the overall capacitance of the device.

26 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as herein disclosed and more particularly claimed below.

CLAIMS:

What is claimed is:

1. A method for improving a dual damascene etching process to block the out diffusion of nitrogen containing photoresist contaminating species to avoid photoresist poisoning in a semiconductor manufacturing process comprising the steps of: providing a semiconductor wafer having a process surface including a via opening extending through a semiconductor wafer thickness portion including an uppermost dielectric anti-reflectance coating (DARC) layer and an underlying dielectric insulating layer to make closed communication with an underlying conductive region; blanket depositing a polymeric resinous layer over the DARC layer to include filling the via opening; curing the polymeric resinous layer by exposing the polymeric resinous layer to at least one of thermal or photonic energy to initiate polymer cross linking; chemically mechanically polishing (CMP) the polymeric resinous layer to substantially remove the polymeric resinous layer thickness above the via opening level to expose the DARC layer and form a via plug substantially filling the via opening; forming a photolithographically patterned photoresist layer over the DARC layer; and, forming a trench line opening overlying and encompassing the via opening to form a dual damascene opening according to a plasma etching process while leaving at least a portion of the via plug in place.

2. The method of claim 1, wherein the DARC layer is selected from the group consisting of silicon oxynitride and titanium nitride.

3. The method of claim 1, wherein the polymeric resinous layer is an I-line novalac resin.

4. The method of claim 1, wherein the polymeric resinous layer is photo-inactive during the step of forming a photolithographically patterned photoresist layer.

5. The method of claim 1, wherein the photolithographically patterned photoresist layer comprises a DUV photoresist including a photogenerated acid photoactive to an activating source of radiation less than about 250 nm.

6. The method of claim 1, wherein the dielectric insulating layer has a dielectric constant of less than about 3.0 comprising a porous material having

interconnecting pores.

7. The method of claim 1, further comprising the step of removing the photolithographically patterned photoresist layer and a remaining portion of the via plug according to at least one of a plasma ashing process and a wet chemical stripping process.

8. The method of claim 1, wherein the step of etching the trench opening comprises using a plasma having a carbon to fluorine ratio of at least about 4.

9. A method for blocking out diffusion of nitrogen containing photoresist contaminating species to improve trench patterning and etching in a dual damascene process comprising the steps of: providing a semiconductor wafer having a process surface including a via opening extending through a semiconductor wafer thickness portion including an uppermost DARC layer and at least a portion of an underlying dielectric insulating layer; blanket depositing a flowable polymeric resinous layer having an average molecular weight of from about 10,000 to about 90,000 over the DARC layer to include filling the via opening; curing the flowable polymeric resinous layer by exposing the polymeric resinous layer to at least one of thermal or photonic energy to initiate polymer cross linking; chemically mechanically polishing (CMP) the polymeric resinous layer according to an oxide CMP process to substantially remove the polymeric resinous layer thickness to expose the DARC layer and form a via plug substantially filling the via opening; providing a photolithographically patterned photoresist layer over the process surface for etching a trench line opening overlying and encompassing the via opening; etching the trench opening according to a plasma etching process to extend through the DARC layer and a thickness portion of the dielectric insulating layer while leaving the via plug in place; and, removing the photolithographically patterned photoresist layer and the via plug according to at least one of a plasma ashing process and a wet chemical stripping process.

10. The method of claim 9, wherein the DARC layer includes at least one of silicon oxynitride and titanium nitride.

11. The method of claim 7, wherein the polymeric resinous layer includes an I-line novalac resin.

12. The method of claim 7, wherein the polymeric resinous layer includes at least one of aliphatic urethane acrylates; aliphatic urethane diacrylates; aliphatic urethane triacrylates; hexafunctional aliphatic urethane acrylates; hexafunctional aromatic urethane acrylates; trifunctional aromatic urethane acrylates, aromatic urethane acrylates; urethane methacrylates; epoxy acrylates; epoxy methacrylates; polybutadiene dimethylacrylates; diacrylates of bisphenol-A epoxy resins; modified bisphenol-A epoxy acrylate resins; novolac epoxy acrylates; modified epoxy acrylates; partially acrylated bisphenol-A epoxy resins; bisphenol-A epoxy diacrylates; polyester resins; cycloaliphatic epoxide resins; modified cycloaliphatic epoxides; aliphatic polyols; partially acrylated bisphenol-A epoxy resins; and cycloaliphatic diepoxides.

13. The method of claim 7, wherein the photolithographically patterned photoresist layer is photoactive to an activating source of radiation less than about 250 nm.

14. The method of claim 7, wherein the dielectric insulating layer has a

dielectric constant of less than about 3.0 including interconnecting pores greater than about 3 Angstroms.

15. The method of claim 9, wherein the step of etching the trench opening comprises using a plasma having a carbon to fluorine ratio of at least about 4.

16. The method of claim 9, wherein the oxide CMP process comprises an oxide polishing slurry having an abrasive material selected from the group consisting of silica (SiO.sub.2), alumina (Al.sub.2 O.sub.3), ceria (CeO.sub.2), titania (TiO.sub.2), manganese oxide (MnO.sub.2), and zirconia (ZrO.sub.2).

17. The method of claim 16, wherein the abrasive material comprises about 1 weight percent to about 20 weight percent of the oxide polishing slurry.

18. The method of claim 9, wherein the oxide CMP process comprises endpoint detection of the DARC layer.

19. The method of claim 9, wherein a second curing process is carried out following the oxide CMP process.

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L3: Entry 2 of 5 File: USPT Sep 16, 2003

US-PAT-NO: 6620745
DOCUMENT-IDENTIFIER: US 6620745 B2

TITLE: Method for forming a blocking layer

DATE-ISSUED: September 16, 2003

INVENTOR-INFORMATION:

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APPL-NO: 10/ 051589 [PALM]
DATE FILED: October 19, 2001

INT-CL: [07] H01 L 21/31

US-CL-ISSUED: 438/787; 438/765
US-CL-CURRENT: 438/787; 438/765

FIELD-OF-SEARCH: 438/765, 438/553, 438/695, 438/787-788, 438/778

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	6066577	May 2000	Cooney et al.	438/787
☐	6127285	October 2000	Nag	438/788
☐	6413879	July 2002	Maeda	438/758

ART-UNIT: 2818

PRIMARY-EXAMINER: Nelms; David

ASSISTANT-EXAMINER: Vu; David

ATTY-AGENT-FIRM: Tung & Associates

ABSTRACT:

A method is provided for forming a blocking layer in a multilayer semiconductor device for blocking diffusion of a chemical species including the steps of providing an insulating layer including a target surface for forming a metal nitride layer thereon said insulating layer forming a portion of a multilayer semiconductor device; treating the target surface with an RF generated plasma to cause a density increase over a thickness adjacent to and including a target surface sufficient to reduce a diffusion rate of chemical species therethrough; forming at least one metal nitride layer over the target surface; and, carrying out a photolithographic process wherein the surface of the at least one metal nitride layer is patterned for etching.

20 Claims, 3 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

BRIEF SUMMARY:

1 FIELD OF THE INVENTION

2 This invention generally relates to methods for forming blocking layers and more particularly to a method for forming a blocking layer to reduce a diffusion rate of a chemical species thereby improving a photolithographic process.

3 BACKGROUND OF THE INVENTION

4 In semiconductor fabrication, various layers of insulating material, semiconducting material and conducting material are formed to produce a multilayer semiconductor device.

5 Since the introduction of semiconductor devices, the size of semiconductor devices has been continuously shrinking, resulting in smaller semiconductor chip size and increased device density on the chip. One of the limiting factors in the continuing evolution toward the smaller device size and higher density has been the interconnect area needed to route interconnect lines between devices. As a way to overcome such limitation, multilayer interconnection systems with increasingly smaller features have been implemented using shared interconnect lines between two or more layers.

6 The layers are patterned to create features that taken together, form elements such as transistors, capacitors, and resistors. These elements are then interconnected to achieve a desired electrical function, thereby producing an integrated circuit (IC) device. The formation and patterning of the various device layers are achieved using conventional fabrication techniques, such as oxidation, implantation, deposition, epitaxial growth of silicon, photolithography, etching, and planarization.

7 One such process for forming a series of interconnected multiple layer devices, for example, is a damascene or dual damascene process. Although there are several different manufacturing methods for manufacturing damascene structures, all such methods employ a series of photolithographic masking and etching steps, typically by a reactive ion etch (RIE). One exemplary process, for example, is known in the art as a via-first-trench last process. Typically a conventional photolithographic process using a photoresist layer is first used to pattern and expose an etching mask which is used for etching via openings through an insulating inter-metal dielectric (IMD) layer. Subsequently a similar process is used to define trench openings for metal interconnect lines in an insulating metallization layer that are formed substantially over the via openings. The via opening and trench openings are subsequently filled with metal to form metallization vias and metal interconnect lines, respectively. The surface may then be planarized by conventional techniques, such as chemical mechanical polishing (CMP) to better define the metal interconnect lines and prepare the substrate for further processing.

8 Referring to FIG. 1, typically, an insulating layer (IMD) 12 layer is formed over a metallization layer 10. Prior to forming the IMD layer 12, an etch stop layer 14A, for example, silicon nitride (SiN) or silicon carbide (SiC) is formed over the metallization layer 10. Another etch layer stop layer 14B is then formed over IMD layer 12. Prior to forming via openings 18A, 18B, and 18C, dielectric anti-reflective coating (DARC) layer 16 is formed over the etching stop layer 14B prior to depositing a photoresist coating 20 for carrying out a photolithographic process used for patterning and subsequently etching by, for example, a reactive ion etch (RIE) the via openings 18A, 18B, and 18C. The DARC layer 16 reduces the effect of light reflection undesirably exposing the photoresist overlayer 20 used for defining via openings 18A, 18B, and 18C. Light reflection (scattering) from, for example, the IMD layer 12 surface, etching stop layer 14B surface, and their respective interfaces, can cause undesired light exposure of the overlying photoresist layer 20 during photolithographic masking and patterning steps in the formation of via openings 18A, 18B, and 18C. As a result, upon development and removal of the exposed photoresist the phenomenon of undercutting (removing photoresist exposed by reflected light at the base of the photoresist layer) will detrimentally affect the design integrity of the manufactured device.

9 As feature sizes in etching process have become increasingly smaller, photolithographic processes hâve been required to use photoresist activating light (radiation) of smaller wavelength. Typically a deep ultraviolet (DUV) activating light source with wavelength less than about 250, but more typically, from about 193 nm to about 230 nm is used. Exemplary DUV photoresists used, for example, have included, PMMA and polybutene sulfone.

10 Many processes use a metal nitride as a DARC (dielectric anti-reflective coating) such as silicon oxynitride (SiON), silicon nitride SiN, or titanium nitride TiN. Typically, the method of choice for depositing these metal nitride layers is a CVD process where for example, a metal-organic precursor together with nitrogen (and oxygen in the case of SiON) is deposited on a substrate surface, to form a metal nitride. Silicon oxynitride DARC, has been widely used for DUV (deep ultraviolet) lithography because of its tunable refractive index and high etch selectivity to resist.

11 One problem affecting DUV photoresist processes has been the interference of residual nitrogen-containing species with the DUV photoresist. Residual nitrogen-containing contamination is one of the greater concerns in the use or application of metal nitride films such as SiN as etch stops and, for example,

silicon oxynitride as a DARC. For example, nitrogen radicals created due to the presence of nitrogen containing species, such as amines, interfere, with chemically amplified resists by neutralizing the acid catalyst, and rendering that portion of the photoresist insoluble in the developer. As a result, residual photoresist may a remain on the edges and walls of features, affecting subsequent etching or metal filling processes and altering design constraints.

12 Another aspect of advances in semiconductor device processing technology that exacerbates the problem is the increasing use of low-k (low dielectric constant)insulating materials that make up the bulk of a multilayer device. In order to reduce signal delays caused by parasitic effects related to the capacitance of insulating layers, for example, IMD layers, incorporation of low-k materials have become standard practice as semiconductor feature sizes have diminished. Many of the low-k materials are designed with a high degree of porosity to allow the achievement of lower dielectric constants. An exemplary low-k material is, for example, carbon doped silicon dioxide (C-oxide) which has a dielectric of about 3 or lower and density of about 1.3 g/cm.sup.3 compared to dielectric constants of about 4.1 and a density of about 2.3 g/cm.sup.3 for silicon dioxides (e.g., un-doped TEOS). A shortcoming of porous low-k materials is that they readily absorb and provide diffusion pathways for chemical species.

13 As a result, amine and nitrogen-containing species remaining in, for example, a SiON DARC, may readily diffuse into an underlying or overlying IMD layer, thereby becoming potentially available for causing interfering effects with a subsequent photoresist process. The contaminating nitrogen-containing species may diffuse back out of the IMD layer during a photoresist process causing residual photoresist to remain after development thereby altering resist profiles by, for example, remaining deposited on feature edges and sidewalls.

14 There is therefore a need in the semiconductor processing art to develop a method whereby residual nitrogen-containing species in for example, DARC layers, are prevented from diffusing into insulating materials, for example, IMD layers, especially where the IMD layers include a low-k material.

15 It is therefore an object of the invention to provide a method whereby residual nitrogen-containing species in for example, DARC layers, are blocked from diffusing into insulating materials, for example, IMD layers, especially where the insulating material is a low-k material while overcoming other shortcomings and deficiencies in the prior art.

16 SUMMARY OF THE INVENTION

17 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a method for forming a blocking layer to reduce a diffusion rate of a chemical species thereby improving a photolithographic process.

18 In a first embodiment according to the present invention, a method if provided for forming a blocking layer in a multilayer semiconductor device for blocking diffusion of a chemical species including the steps of: providing an insulating layer comprising a target surface for forming a metal nitride layer thereon said insulating layer forming a portion of a multilayer semiconductor device; treating the target surface with an RF generated plasma to cause a density increase over a thickness adjacent to and including a target surface sufficient to reduce a diffusion rate of a chemical species therethrough;

forming at least one metal nitride layer over the target surface; and, carrying out a photolithographic process wherein the surface of the at least one metal nitride layer is patterned for etching.

19 In related embodiments, the target surface comprises a silicon oxide. Further, the silicon oxide further comprises a low-k material with a dielectric constant of less than about 3.5. Further yet, the low-k material includes carbon doped silicon dioxide.

20 In another related embodiment, the at least one metal ergo nitride layer includes an etch stop layer and a dielectric anti-reflectance coating (DARC) layer. Further, the etch stop layer is selected from the group consisting of silicon nitride, silicon oxynitride, and titanium nitride. Further yet, the DARC layer is selected from the group consisting of silicon nitride, silicon oxynitride, and titanium nitride.

21 In another related embodiment, the photolithographic process comprises photogeneration of a nitrogen containing radical species within a photoresist.

22 In yet another related embodiment, the density increase comprises a physical process including ions in the RF generated plasma impacting on the target surface. Further, the physical process is carried out prior to a chemical process whereby ions in the RF generated plasma chemically react with the target surface.

23 In another embodiment, the density increase comprises a chemical process whereby ions in the RF generated plasma chemically react with the target surface. Further, the ions include oxygen ions and the target surface includes silicon oxide whereby oxygen is incorporated into the target surface.

DRAWING DESCRIPTION:

These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional representational view of a portion of a multilayer semiconductor device according to the prior art.

FIG. 2 is a cross-sectional representational view of a portion of a multilayer semiconductor device.

FIG. 3 is a cross-sectional representational view of a portion of a multilayer semiconductor device at a stage in the manufacture of a multilayer semiconductor device according to the present invention.

DETAILED DESCRIPTION:

1 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

2 The method and apparatus according to the present invention is more clearly

described by referring to FIG. 2.

3 FIG. 2 is a cross sectional view of a portion of a dual damascene structure showing a trench opening 220 overlying a via openings 218A, 218B, and 218C. Both the trench opening and via openings are, for example, etched by a reactive ion etch (RIE) process into their respective insulating layers. The insulating layer comprising the via openings is herein referred to as an IMD layer 214 and the insulating layer comprising the trench opening defining a metallization line is referred to as a metallization layer 216. Although several different insulating materials may be used in either the IMD layer 214 or the metallization layer 216 including silicon dioxide, preferably a low-k (low dielectric constant material) is used, for example, carbon doped silicon oxide (C-oxide). It will be appreciated that other low-k materials may be used and that the method according to the present invention is likewise applicable to those materials, particularly if they are porous materials. It will also be appreciated that the amount of carbon doping may be varied in both the IMD layer 214 and the metallization layer 216. It will be further appreciated that the present invention is described by reference only to an exemplary portion of a multilayer device comprising multiple IMD and metallization layers, it being understood that the invention applies to the entire multilayer device.

4 Although there are several different processes that are well known in the art in creating a multiple layer semiconductor device such as, for example, a dual damascene process, a typical process will require at least two photolithographic and etching steps; one for the defining and etching the via openings in the IMD layer 214 and one for defining and etching the trench openings in the metallization layer 216.

5 In a typical dual damascene process, still with reference to FIG. 2, a barrier layer (etch stop) 204A is formed over an underlying metallization contact, for example, a metallization line 202, for acting as a barrier layer to protect the metallization line 202 and as an etch stop in a subsequent etching process of the overlying IMD layer 214 to form via openings 218A, 218B, and 218C. The etch stop layer 204A is preferably silicon nitride (SiN) or silicon carbide (SiC). An IMD layer 214 is then formed over the etch stop layer 204A. The silicon nitride layer 204 may be deposited by a PECVD or LPCVD process by reacting silane (SiH.sub.4) or an amine-containing metal-organic precursor with ammonia (NH.sub.3) or nitrogen under conditions that are well known in the art.

6 A DARC layer 208 is deposited over the IMD layer to reduce undesired light reflections in a subsequent photolithographic patterning process to define, for example, via openings. Another etch stop layer 204B may be deposited over the IMD layer 214 prior to forming the DARC layer. Preferably, the DARC layer 208 is silicon oxynitride (SiON), but may be other metal nitrides, such as Titanium nitride. The SiON may be deposited by a (chemical vapor deposition (CVD) process including for example, PECVD (plasma enhanced CVD), LPCVD (low pressure CVD), or HDPCVD (high density plasma CVD) by reacting silane (SiH.sub.4) or an amine-containing metal-organic precursor with ammonia (NH.sub.3) or nitrogen together with oxygen under conditions that are well-known in the art.

7 In a high density plasma (HDPCVD) process to deposit metal nitrides including SiON, for example, processing conditions may include, any frequency and any combination of RF powers at a range of between 50 watts and about 5,000 watts and at pressure ranges of between about 0.1 mTorr and about 20 mTorr. The bias power for Ar sputtering is between the range of 0 watts and about 4,000 watts. Preferably, O.sub.2 gas or, N.sub.2 O is used as an oxygen source for the DARC. For example, the O.sub.2 gas flow rate during deposition is between

about 1 sccm and about 500 sccm, and the N.sub.2 flow rate during deposition is between about 1 sccm and about 500 sccm.

8 Depending on the dual damascene process the via openings may be defined by a photolithographic process and etched in the IMD layer prior to depositing an insulating layer to form the metallization layer. Alternatively, via openings may be defined and etched after forming the metallization layer and etching the trench opening. In either case a photolithographic process whereby photoresist is applied to the surface to be patterned, for example, by spin-coating, an exposed to activating radiation is carried out for patterning both the IMD layer and metallization layer surfaces for etching via openings or trench openings, respectively.

9 Preferably, a deep ultraviolet (DUV) activating radiation source of less than 250 nm, but more preferably, about 193 nm, is used to expose the photoresist to form the etching pattern. Correspondingly, a DUV photoresist is used for the patterning process. Preferably the photoresist is a chemically amplified resist including a photogenerated acid. There are several suitable commercially available photoresists including for example, PMMA and polybutene sulfone.

10 According to the present invention, referring to FIG. 3 a blocking layer 302 is formed over the insulating layers, for example, the IMD layer 304, prior to forming a DARC layer and patterning and etching the via openings. The IMD layer 304 is again formed over an etch stop layer 306 and a metal contact region in a metallization layer 308. According to the present invention, the blocking layer 302 comprises a densified upper portion of the IMD layer 304 including an insulating material such as, for example, C-oxide. According to the present invention, the surface of the IMD layer material density is increased by an RF generated plasma treatment to form the blocking layer 302. It will be appreciated that the invention as described may apply to the insulating layer including the trench opening 220 in FIG. 2 prior to forming another IMD layer 214 over the metallization layer 216.

11 In one aspect of the invention, in the plasma surface densification treatment, inert gases such as Ar or He are used and densification occurs by a physical impacting process. The ions making up the plasma increase the density of the upper surface (302 in FIG. 3) of the insulating layer (target surface) exposed to the plasma, for example, the IMD layer, by energy and momentum transferred by the plasma ions impacting the surface of the IMD layer (304 in FIG. 3). Preferably, plasma conditions are such that the insulating material density increases at the surface over a depth of about 10 Angstroms to about 150 Angstroms. For example, the density of C-oxide is preferably increased within a range of about 1.3 g/cm.sup.3 to about 2.3 g/cm.sup.3. More preferably, the density of the insulating material at the surface is increased by about 10% to about 50% over a depth of about 10 Angstroms to about 150 Angstroms. It will be appreciated that the degree of densification will vary over the depth adjacent to the surface. For example, there is a greater degree of energy and momentum transfer by impacting plasma ions as in that portion of the insulating material closer to the surface

12 The degree of densification will depend on the energy of the plasma and the processing time. Exemplary processing variables include a gas flow rate from about 1 to about 5000 sccm, more preferably, about 500 to about 1500 sccm; a pressure from about 0.1 to about 100 Torr, more preferably, about 1 to about 50 Torr; and an RF power of about 10 to about 5000 Watts, more preferably, from about 500 to about 1000 Watts. Further, a biasing power may be used with a range of about 0 to about 4000 Watts.

13 According to another aspect of the invention, oxygen may be substituted for the inert gases or combined with them. Preferably the oxygen is combined with inert gases to allow for a greater range of processing pressures. In an oxygen containing plasma, both a physical and chemical densification process may contribute to the densification of the target surface. The oxygen containing plasma initiates a reaction in for example, the C-oxide, to oxidize the target surface by forming silicon dioxide by reaction with, for example, the dangling silicon surface bonds or replacement of residual silicon hydrogen bonds remaining on the target surface after the insulating layer deposition process. In addition, the target surface densification may occur by a physical process whereby energy and momentum is transferred to the target surface by impacting ions generated in the plasma process. Exemplary processing conditions include a gas flow rate from about 1 to about 5000 sccm, more preferably, about 500 to about 1500 sccm; a pressure from about 0.1 to about 100 Torr, more preferably, about 1 to about 50 Torr; and an RF power of about 10 to about 5000 Watts, more preferably, from about 500 to about 1000 Watts. Further, a biasing power may be used with a range of about 0 to about 4000 Watts.

14 In another aspect of the invention, the target surface is first oxidized by a plasma treatment with an oxygen containing plasma source and then further densified by a plasma treatment with an inert gas source. Alternatively, the target surface may be first densified by a plasma treatment with an inert gas source and then oxidized by a plasma treatment with an oxygen containing plasma source. Preferably, nitrogen containing gases are substantially absent from the plasma gas sources.

15 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.

CLAIMS:

What is claimed is:

1. A method of forming a blocking layer in a multilayer semiconductor device for blocking diffusion of a chemical species comprising the steps of: providing an insulating layer comprising a target surface for forming a metal nitride layer thereon said insulating layer forming a portion of a multilayer semiconductor device; treating the target surface with an RF generated plasma to cause a density increase over a thickness adjacent to and including a target surface sufficient to reduce a diffusion rate of a nitrogen containing chemical species therethrough; forming at least one metal nitride layer over the target surface; and carrying out a photolithographic process wherein the surface of the at least one metal nitride layer is patterned for etching.

2. The method of claim 1, wherein the target surface comprises a silicon oxide.

3. The method of claim 2, wherein the oxide further comprises a low-k material with a dielectric constant of less than about 3.5.

4. The method of claim 3, wherein the low-k material comprises carbon doped silicon dioxide.

5. The method of claim 1, wherein the at least one metal nitride layer

includes an etch stop layer and a dielectric anti-reflectance coating (DARC) layer.

6. The method of claim 5, wherein the etch stop layer is selected from the group consisting of silicon nitride, silicon oxynitride, and titanium nitride.

7. The method of claim 5, wherein the DARC layer is selected from the group consisting of silicon nitride, silicon oxynitride, and titanium nitride.

8. The method of claim 1, wherein the photolithographic process comprises photogeneration of a nitrogen containing radical species within a photoresist.

9. The method of claim 1, wherein the density increase comprises a physical process including ions in the RF generated plasma impacting on the target surface.

10. The method of claim 9, wherein the physical process is carried out prior to a chemical process whereby ions in the RF generated plasma chemically react with the target surface.

11. The method of claim 1, wherein the density increase comprises a chemical process whereby ions in the RF generated plasma chemically react with the target surface.

12. The method of claim 11, wherein the ions include oxygen ions and the target surface includes silicon oxide whereby oxygen is incorporated into the target surface.

13. The method of claim 11, wherein the chemical process is carried out prior to a physical process including ions in the RF generated plasma impacting on the target surface.

14. The method of claim 1, wherein the density increase is within a range of about 10 percent to about 50 percent.

15. The method of claim 1, wherein the density increase occurs over a range of about 10 angstroms to about 150 Angstroms.

16. The method of claim 1, wherein the density increase varies over the thickness from about wherein the density varies over the thickness from about 2.3 g/cm.sup.3 to about 1.3 g/cm.sup.3.

17. The method of claim 1, wherein the RF generated plasma includes at least one gas source selected from the group consisting of Argon, Helium, Xenon, and oxygen.

18. The method of claim 1, wherein the chemical species is a nitrogen containing species.

19. The method of claim 1, wherein the density increase is carried out under process conditions comprising: a gas flow rate from about 1 sccm to about 5000 sccm; a pressure from about 0.1 Torr to about 100 Torr; and an RF power of about 10 Watts to about 5000 Watts.

20. The method of claim 1, wherein the density increase is carried out under process conditions comprising: a gas flow rate from about 500 sccm to about

1500 sccm; a pressure from about 1 Torr to about 50 Torr; and an RF power of about 500 Watts to about 1000 Watts.

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L3: Entry 3 of 5 File: USPT Oct 1, 2002

US-PAT-NO: 6458689
DOCUMENT-IDENTIFIER: US 6458689 B2

TITLE: Use of PE-SiON or PE-Oxide for contact or via photo and for defect reduction with oxide and w chemical-mechanical polish

DATE-ISSUED: October 1, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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Shih; Tsu	Hsin-Chu			TW
Yen; Anthony	Hsin-Chu			TW
Twu; Jih-Chuyng	Chung-ho			TW

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Taiwan Semiconductor Manufacturing Company	Hsin-Chu			TW	03

APPL-NO: 09/ 818714 [PALM]
DATE FILED: March 28, 2001

PARENT-CASE:

This is a division of patent application Ser. No. 09/263,563, filing date Mar. 8, 1999. U.S. Pat. No. 6,228,760. The Use of Pre-Sion Or Pe-Oxide For Contact Or Via Photo And For Perfect Reduction With Oxide And W Chemical Mechanical Polish, assigned to the same assignee as the present invention.

INT-CL: [07] H01 L 21/476

US-CL-ISSUED: 438/631; 438/633, 438/636
US-CL-CURRENT: 438/631; 438/633, 438/636

FIELD-OF-SEARCH: 438/618, 438/620-640, 438/691-692

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5354712	October 1994	Ho et al.	437/195
☐	5674784	October 1997	Jang et al.	437/195
☐	5766974	June 1998	Sardella et al.	437/195
☐	5767018	June 1998	Bell	438/696
☐	5886410	March 1999	Chiang et al.	
☐	6077784	June 2000	Wu et al.	
☐	6114325	September 2000	Foote et al.	

ART-UNIT: 2812

PRIMARY-EXAMINER: Tsai; Jey

ATTY-AGENT-FIRM: Saile; George O. Ackerman; Stephen B. Stoffel; William J.

ABSTRACT:

A method forming a protective (SiON or PE-Ox) dielectric anti-reflective coating (DARC) over a dielectric layer after a chemical-mechanical polish dielectric layer planarization process and before a chemical-mechanical polish of a conductive layer used in a contact or via plug formation. A dielectric layer is chemical-mechanical polished thereby creating microscratches in the dielectric layer. The invention's protective SiON or PE-OX DARC layer is formed over the dielectric layer whereby the protective SiON or PE-OX DARC layer fills in the microscratches. A first opening is etched in he protective layer and the dielectric layer. A conductive layer is formed over the protective layer and fills the first opening. The conductive layer is chemical-mechanical polished to remove the conductive layer from over the protective layer and to form an interconnect filling the first opening. The protective SiON or PE-OX DARC layer is used as a CMP stop thereby preventing microscratches in the dielectric layer.

3 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BRIEF SUMMARY:

1 BACKGROUND OF INVENTION

2 1) Field of the Invention

3 This invention relates generally to fabrication of contact or via holes using an Anti-Reflection Coating and chemical-mechanical polishing processes in semiconductor devices and more particularly to the fabrication of an Anti-Reflection Coating composed of Silicon oxynitride (SiON) and chemical-mechanical polish processes used in making contact holes or via holes in ILD or IMD dielectric layers.

4 2) Description of the Prior Art

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L3: Entry 4 of 5 File: USPT May 8, 2001

US-PAT-NO: 6228760
DOCUMENT-IDENTIFIER: US 6228760 B1
** See image for Certificate of Correction **

TITLE: Use of PE-SiON or PE-OXIDE for contact or via photo and for defect reduction with oxide and W chemical-mechanical polish

DATE-ISSUED: May 8, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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Jang; Syun-Ming	Hsin-Chu			TW
Shih; Tsu	Hsin-Chu			TW
Yen; Anthony	Hsin-Chu			TW
Twu; Jih-Churng	Hsin-Chu			TW

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Taiwan Semiconductor Manufacturing Company	Hsin-Chu			TW	03

APPL-NO: 09/ 263563 [PALM]
DATE FILED: March 8, 1999

INT-CL: [07] H01 L 21/4763

US-CL-ISSUED: 438/636; 438/637, 438/634, 438/672, 438/680, 438/970
US-CL-CURRENT: 438/636; 438/634, 438/637, 438/672, 438/680, 438/970

FIELD-OF-SEARCH: 438/636, 438/637, 438/672, 438/680, 438/970, 438/634

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5354712	October 1994	Ho et al.	437/195
☐	5674784	October 1997	Jang et al.	437/195
☐	5766974	June 1998	Sardella et al.	437/195
	5767018	June 1998	Bell	438/696

☐	6114235	September 2000	Foote et al.	438/636

ART-UNIT: 282

PRIMARY-EXAMINER: Niebling; John F.

ASSISTANT-EXAMINER: Zarneke; David A.

ATTY-AGENT-FIRM: Saile; George O. Ackerman; Stephen B. Stoffel; William J.

ABSTRACT:

A method forming a protective (SiON or PE-Ox) dielectric anti-reflective coating (DARC) over a di electric layer after a chemical-mechanical polish dielectric layer planarization process and before a chemical-mechanical polish of a conductive layer used in a contact or via plug formation. A dielectric layer is chemical-mechanical polished thereby creating microscratches in the dielectric layer. The invention's protective SiON or PE-OX DARC layer is formed over the dielectric layer whereby the protective SiON or PE-OX DARC layer fills in the microscratches. A first opening is etched in he protective layer and the dielectric layer. A conductive layer is formed over the protective layer and fills the first opening. The conductive layer is chemical-mechanical polished to remove the conductive layer from over the protective layer and to form an interconnect filling the first opening. The protective SiON or PE-OX DARC layer is used as a CMP stop thereby preventing microscratches in the dielectric layer.

7 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BRIEF SUMMARY:

1 BACKGROUND OF INVENTION

2 1) Field of the Invention

3 This invention relates generally to fabrication of contact or via holes using an Anti-Reflection Coating and chemical-mechanical polishing processes in semiconductor devices and more particularly to the fabrication of an Anti-Reflection Coating composed of Silicon oxynitride (SiON) and chemical-mechanical polish processes used in making contact holes or via holes in ILD or IMD dielectric layers.

4 2) Description of the Prior Art

5 Chemical-mechanical polish (CMP) planarization processes are used to level dielectric layers and to polish down metal layer in semiconductor devices. However, these CMP process can create microscratches in dielectric layers that degrade photolithographic performance and create defects. The inventor (s) have found the following problems as described below and in FIGS. 8A to 8D. This is not prior art for the patentability of the invention.

6 FIG. 8A shows the chemical-mechanical polishing 209 of a dielectric layer 214 overlying a metal line 211 on a substrate 10. FIG. 8B shows the microscratches 216 the inventor has noticed after the chemical-mechanical polish.

7 Next, an organic bottom anti-reflective coating (BARC) layer 218 and a photoresist layer 224 are formed over the dielectric layer 214 and the microscratches 216. The organic BARC layer 218 and a photoresist layer 224 are exposed to create a photoresist opening 225 (shown as dashed lines).

8 A problem the inventor has noticed is that the microscratches create reflections that degrade the photoresist pattern.

9 Next, a via hole is etched in the dielectric layer 214 as shown in FIG. 8C. The photoresist layer is removed.

10 As shown in FIG. 8C, a barrier layer 228 and metal layer 230 are formed over the dielectric layer and fill the via hole. The barrier layer and metal layer fill in some of the microscratches.

11 FIG. 8D shows the CMP of the metal layer and barrier layer to form the metal plug 323. However, the microscratches 216 are filled with metal and barrier layer 228. These filled microscratches create defects, short with overlying conductive lines and create photo defects.

12 Moreover, new microscratches 245 are formed in the dielectric layer by the metal CMP. These new metal chemical-mechanical polish created microscratches 245 cause similar problems.

13 Therefore, there is a need for a method to prevent microscratches in dielectric layers formed during contact/via hole formation and contact plug/via plug CMP processes.

14 The importance of overcoming the various deficiencies noted above is evidenced by the extensive technological development directed to the subject, as documented by the relevant patent and technical literature. The closest and apparently more relevant technical developments in the patent literature can be gleaned by considering U.S. Pat. No. 5,766,974 (Sardella)--Method of making a dielectric structure for facilitating overetching of metal without damage to inter-level dielectric--that shows an integrated circuit fabrication with a thin layer of oxynitride atop the interlevel dielectric, to provide an etch stop to withstand the overetch of the metal layer. U.S. Pat. No. 5,767,018 (Bell) shows polysilicon etch process using an ARC layer. U.S. Pat. No. 5354712 (Ho)Method for forming interconnect structures for integrated circuits--teaches dielectric layer that is chemical-mechanical polished. U.S. Pat. No. 5,674,784 (Jang et al.) shows a method of forming a polish stop for a CMP process.

15 SUMMARY OF THE INVENTION

16 It is an object of the present invention to provide a method of covering microscratches created by a chemical-mechanical polishing of a dielectric layer using a SiON layer.

17 It is an object of the present invention to provide a method provides a method of preventing/filling microscratches in a dielectric layer created by a chemical-mechanical polishing of a conductive layer in a contact or via plug

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L3: Entry 5 of 5 File: USPT Dec 5, 2000

US-PAT-NO: 6156149
DOCUMENT-IDENTIFIER: US 6156149 A

TITLE: In situ deposition of a dielectric oxide layer and anti-reflective coating

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

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ASSIGNEE-INFORMATION:

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Applied Materials, Inc.	Santa Clara	CA			02

APPL-NO: 08/ 852788 [PALM]
DATE FILED: May 7, 1997

PARENT-CASE:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to patent application Ser. No. 08/672,888 entitled "METHOD AND APPARATUS FOR DEPOSITING ANTIREFLECTIVE COATING," having David Cheung, Joe Feng, Judy H. Huang, and Wai-Fan Yau as inventors; Application No 16301-009310/AMAT-1084-P2 entitled "METHOD AND APPARATUS FOR DEPOSITING AN ETCH STOP LAYER," having Judy H. Huang, Wai-Fan Yau, David Cheung, and Chan-Lon Yang as inventors; and Application No 16301-016100/AMAT-1694 entitled "METHOD AND APPARATUS FOR APPLYING AN ANTIREFLECTIVE COATING USING REDUCED DEPOSITION RATES," having David Cheung, Wai-Fan Yau, Joe Feng, Judy H. Huang, and Madhu Deshpande as inventors. All of these applications are assigned to Applied Materials, Inc., the assignee of the present invention, and are hereby incorporated by reference.

INT-CL: [07] B32 B 31/00

US-CL-ISSUED: 156/272.2; 156/274.4, 156/272.6, 118/705, 118/708, 118/712, 118/722, 427/255.7, 427/279, 438/763, 438/784 , 438/788
US-CL-CURRENT: 156/272.2; 118/705, 118/708, 118/712, 118/722, 156/272.6, 156/274.4, 257/E21.029, 427/255.7, 427/279, 438/763, 438/784, 438/788

FIELD-OF-SEARCH: 148/724, 148/725, 148/665, 148/722, 148/723, 148/712, 156/643, 156/272.2, 156/272.6, 438/763, 438/784, 438/788, 118/722, 118/699, 118/705, 118/708, 118/712, 118/50.1, 427/255.7, 427/579

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4998979	March 1991	Nino	134/1
☐	5261961	November 1993	Takasu et al.	118/722
☐	5443646	August 1995	Yamada et al.	118/722
☐	5661093	August 1997	Raui et al.	438/763

ART-UNIT: 174

PRIMARY-EXAMINER: Dixon; Merrick

ATTY-AGENT-FIRM: Townsend & Townsend & Crew

ABSTRACT:

This invention provides a method and apparatus for depositing a two-layer structure, including an antireflective coating and a dielectric layer, without any intervening process steps, such as a cleaning step. The invention is capable of providing more accurate and easier fabrication of structures by reducing inaccuracies caused by the reflection and refraction of incident radiant energy within a photoresist layer used in the patterning of the dielectric layer. Additionally, the antireflective coating of the present invention may also serve as an etch stop layer during the patterning of a layer formed over the antireflective coating.

19 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

BRIEF SUMMARY:

1 BACKGROUND OF THE INVENTION

2 The present invention relates to an apparatus for, and the processing of, semiconductor substrates. In particular, the invention relates to the in situ deposition of dielectric layers and antireflective coatings, and the patterning of such films during substrate processing.

3 Since semiconductor devices were first introduced several decades ago, device geometries have decreased dramatically in size. During that time, integrated circuits have generally followed the two year/half-size rule (often called "Moore's Law"), meaning that the number of devices which will fit on a chip doubles every two years.

4 Today's semiconductor fabrication plants routinely produce devices with feature sizes of 0.5 microns or even 0.35 microns, and tomorrow's plants will be producing devices with even smaller feature sizes.

5 A common step in the fabrication of such devices is the formation of a patterned thin film on a substrate by chemical reaction of gases. When patterning the thin films, it is desirable that fluctuations in line width and other critical dimensions be minimized. Errors in these dimensions can result in variations in device characteristics or open-/short-circuited devices, thereby adversely affecting device yield. Thus, as feature sizes decrease, structures must be fabricated with greater accuracy. As a result, some manufacturers now require that variations in the dimensional accuracy of patterning operations be held to within 5% of the dimensions specified by the designer.

6 These films are often formed by etching away portions of a deposited blanket layer. Modern substrate processing systems employ photolithographic techniques to pattern layers. Typically, such photolithographic techniques employ photoresist or other light-sensitive material deposited on a wafer. A photomask (also known simply as a mask) having transparent and opaque regions embodying the desired pattern is positioned over the photoresist. When the mask is exposed to light, the transparent portions allow for the exposure of the photoresist in those regions, but not in the regions where the mask is opaque. The light causes a chemical reaction in exposed portions of the photoresist (e.g., photosolubilization or polymerization). A suitable chemical, chemical vapor or ion bombardment process is then used to selectively attack either the reacted or unreacted portions of the photoresist. With the remaining photoresist pattern acting as a mask, the underlying layer may then undergo further processing. For example, the layer may be doped or etched, or other processing carried out.

7 Modern photolithographic techniques often involve the use of equipment known as steppers, which are used to mask and expose photoresist layers. Steppers often use monochromatic (single-wavelength) light, enabling them to produce the detailed patterns required in the fabrication of fine geometry devices. As a substrate is processed, however, the topology of the substrate's upper surface becomes progressively less planar. This uneven topology can cause reflection and refraction of the monochromatic light, resulting in exposure of some of the photoresist beneath the opaque portions of the mask. As a result, this uneven surface topology can alter the mask pattern transferred to the photoresist layer, thereby altering the desired dimensions of the structures subsequently fabricated.

8 One phenomenon which may result from these reflections is known as standing waves. When a photoresist layer is deposited on a reflective underlying layer and exposed to monochromatic radiation (e.g., deep ultraviolet (UV) light), standing waves may be produced within the photoresist layer. In such a situation, the reflected light interferes with the incident light and causes a periodic variation in light intensity within the photoresist layer in the vertical direction. Standing-wave effects are usually more pronounced at the deep UV wavelengths used in modern steppers than at longer wavelengths because surfaces of materials such as oxide, nitride, and polysilicon are more reflective at deep UV wavelengths. The existence of standing waves in the photoresist layer during exposure causes roughness in the vertical walls formed when sections of the photoresist layer are removed during patterning, which translates into variations in linewidths, spacing and other critical dimensions.